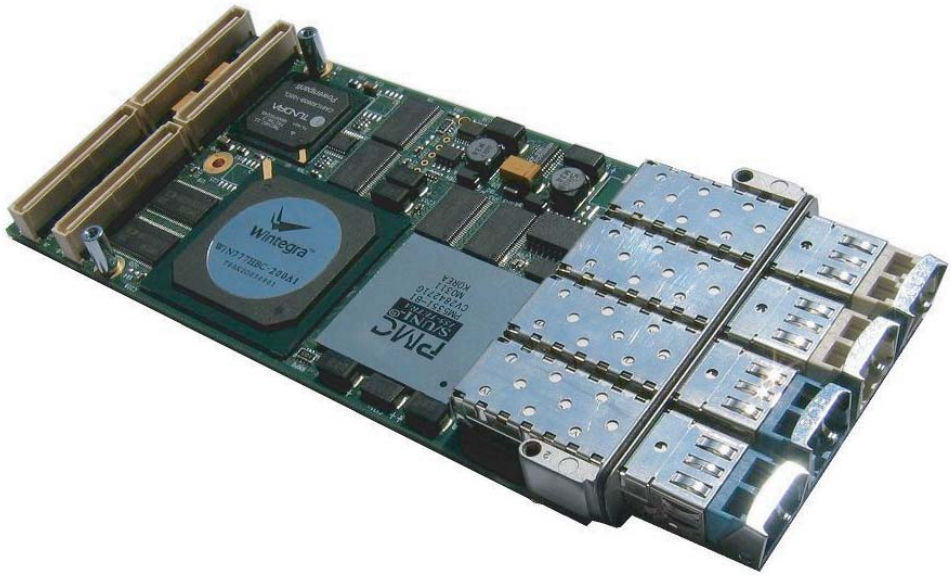
XS-155

Quad STS-3c/STM-1 ATM/POS Interface

Applications

- 3G NodeB, RNC, MSC & SGSN
- Voice over Packet
- Video Streaming
- Broadband Networks
- ATM to IP Gateways
- IPv4 to IPv6 Gateways



Main Features

- ATM AAL0, AAL1, AAL2 & AAL5
- IP version 4 and 6
- Quad OC-3 / STM-1
- PICMG® 2.15 PT4MC
- WinPath™ Network Processor
- On-board 64-bit MIPS 5Kc™
- On-board Switching
- 384 MB SDRAM
- 16 MB Flash EPROM
- 8 KHz Tx and Rx Ref. Clock
- Small Form Pluggable (SFP) Optical Transceivers
- Extensive Software Support
- Linux and VxWorks®

XS-155 is the first member of a family of PCI Telecom Mezzanine Card (PTMC) which offers high-end ATM and IP services at an attractive price. XS-155 provides termination, switching and interworking capabilities from any port to any port.

XS-155 performance and features are ideally suited for applications such as Wireless networking, Voice over Packet, Internet access, Video streaming, and next generation networks.

Using the state of the art Wintegra™'s WinPath™ Network Processor, XS-155 is the perfect interface to handle both ATM and IP simultaneously.

XS-155 on-board 64-bit MIPS processor can run advanced protocols (e.g. 3GPP, SS7, ATM, VoIP) while the Network Processor handles all the data path.

Providing 2.4 Gbps aggregate throughput, XS-155, the industry's first network processor on a PMC, features the highest OC-3/STM-1 port density on the market.

Compliant with IEEE 1386.1 PCI Mezzanine card (PMC) and PICMG 2.15 PCI Telecom Mezzanine Card (PTMC), the XS-155 can be used in cPCI, cPSB, AdvancedTCA™, VME, PC, and proprietary applications.

XS-155 architecture allows to bypass the bottleneck of current systems by handling all the processing on-board and performing segmentation and reassembly locally, which not only allows to offload the CPU on the carrier board but also optimizes bus transfers while doing termination.

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XS-155

Quad STS-3c/STM-1 ATM/POS Interface

ATM

- AAL0, AAL1, AAL2 & AAL5 (1)
- ATM cell switching
- AAL2 CID switching
- Traffic management as per TM 4 .1: CBR, VBR, GFR and UBR
- Per VC queueing
- Dual leaky bucket policing
- Full UNI/NNI VPI/VCI range
- OAM F4 and F5 as per ITU-T I.610

PT4MC

- PICMG® 2.15 fully compliant (3)
- UTOPIA L2 @ 50 MHz
- 8 or 16-bit data bus interface
- Master and slave configuration
- Cell size from 52 to 65 octets
- 8 KHz Tx and Rx reference clock
- Serial port

Network Processor

- Wintegra™ WinPath™ @ 200 MHz
- 128 MBytes Packet SDRAM (4)
- 128 MBytes Parameter SDRAM
- 64-bit / 100 MHz SDRAM
- MIPS 5Kc™ CPU @ 200 MHz
- 4 WinGines
- Communication throughput up to 2.4 Gbps
- Handles more than 18 data path protocols to date
- For more details see www.wintegra.com

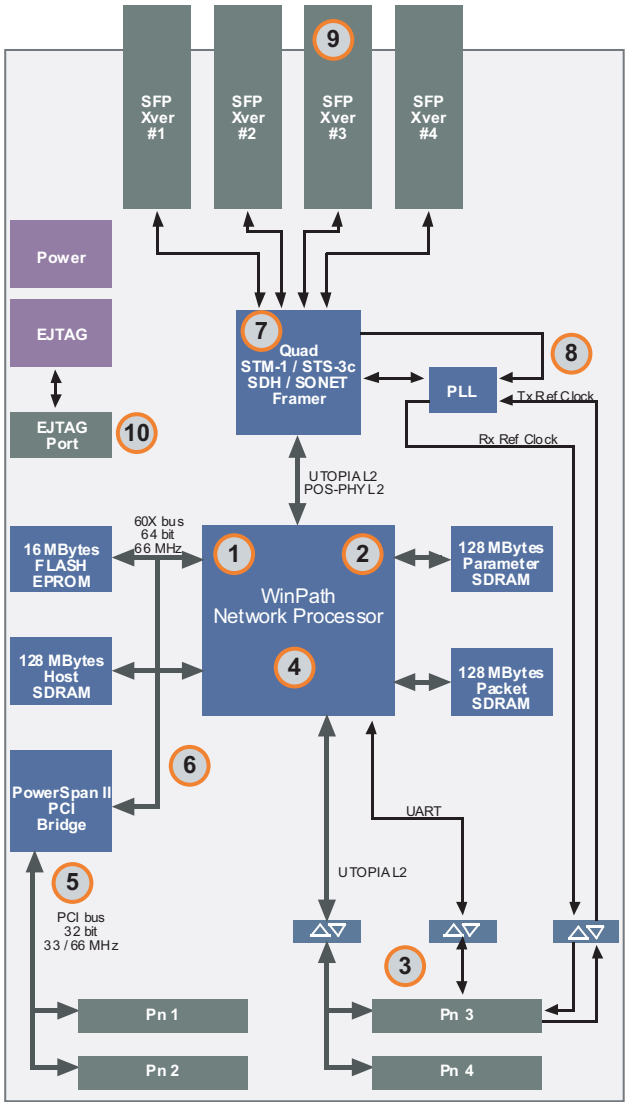
Interworking

- IP routing and forwarding over ATM (RFC 1483/2684/1577)
- IP routing and forwarding over PPP (RFC 1661)
- Multiple fields classification and DiffServ (RFC 2474/2475)
- MPLS tagging/detagging
- L2 interworking between ATM and Ethernet
- Interworking at 750'000 PPS

IP

- IPv4 and IPv6 (2)
- PPP support
- HDLC support up to OC-12 rates
- Parsing of PPP over HDLC frames (RFC 2615 and RFC 1662)
- Packet scheduling

Block Diagram



XALYO SYSTEMS

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Quad STS-3c/STM-1 ATM/POS Interface

System busses

PCI bus (5)

- PCI 2.2 Specification compliant
- 32-bit interface
- 33 / 66 MHz operation
- 3.3 V and 5 V signaling
- Intelligent I2O messaging

Host bus (6)

- PPC 60X @ 66 MHz
- 64-bit interface
- 128 MBytes Host Memory
- 16 MBytes Flash EPROM

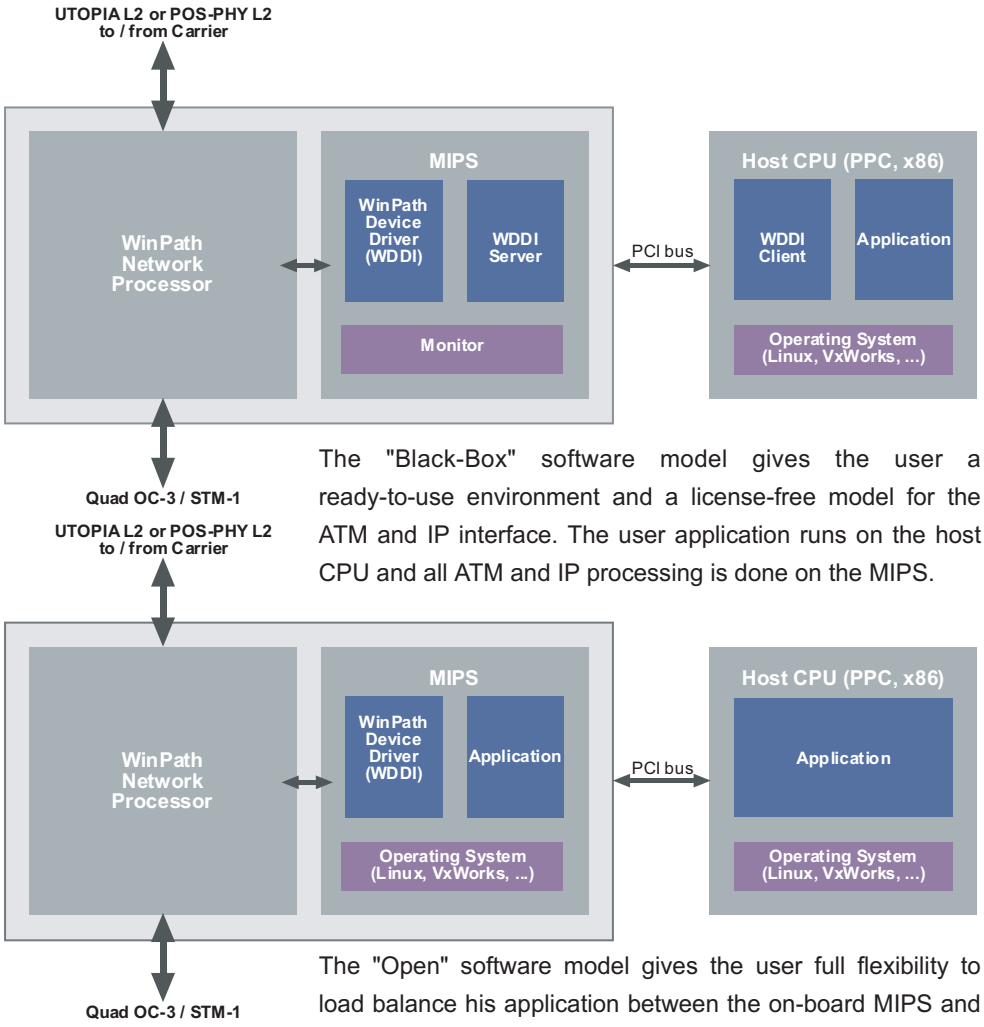
Physical Layer

- Quad STM-1 / STS-3c (7)
- Duplex 155.52 Mbps per port
- STM-1 or STS-3c selectable per port
- ATM (ITU I.432)
- POS (RFC 1619 / RFC 1662)
- APS support (K1, K2 bits)

Telecom Clock

- 8 KHz to 19.44 MHz PLL (8)
- Meets TR62411, ETS300 011 and GR-1244 for Jitter/Wander for Stratum 3 and higher
- 8 KHz selectable from backplane or any STM-1/STS-3c port
- 8 KHz reference output to backplane
- Locks to 8 KHz +/- 100 ppm

Software Model



The "Black-Box" software model gives the user a ready-to-use environment and a license-free model for the ATM and IP interface. The user application runs on the host CPU and all ATM and IP processing is done on the MIPS.

The "Open" software model gives the user full flexibility to load balance his application between the on-board MIPS and the CPU on the carrier card. The WDDI and the BSPs for the different operating systems are available in source code.

Optical Transceivers

- Multisource agreement (MSA) compliant SFP package (9)
- LC duplex receptacle connector
- Hot pluggable electrical interface
- Customers can buy the transceivers directly from their selected suppliers
- One PMC card for all variants: Multimode, singlemode, short, intermediate and long reach

Debug Connector

- 14 points Enhanced JTAG port for debugging (software breakpoints, single step mode) (10)
- Easy to fit optionnal connector

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Quad STS-3c/STM-1 ATM/POS Interface

Specifications

Form factor	PTMC Option 4
Dimensions	74 mm x 149 mm
PCI bus	32-bit, 33 and 66 MHz
Host bus	64-bit, 66 MHz
UTOPIA bus	8 and 16-bit, 50 MHz, L2
POS-PHY bus	8 and 16-bit, 50 MHz, L2
Optical connector	LC duplex
Telecom reference clock	8 Khz
Communication ports	Quad OC-3/STM-1
UART	RS232
Protocols	ATM and IP
Flash memory	16 MBytes, 150 ns
Host memory	128 MBytes, 66 MHz
Parameter memory	128 MBytes, 100 MHz
Packet memory	128 MBytes, 100 MHz
Operating systems	Linux, VxWorks®
Operating temperature	0 to 55°C
Storage temperature	-40 to 85°C
Relative humidity	5% to 90% non-condensing
Altitude	0 to 15'000 ft
Power consumption	10.0 W max
3.3 V	6.0 W max
5.0 V	4.0 W max

Standards compliance

PCI	PCI Local Bus Specification Rev. 2.2
IEEE P1386	CMC: Common Mezzanine Card
IEEE P1386.1	PMC: PCI Mezzanine Card
IEEE 1149.1	JTAG
PICMG® 2.15	PTMC: PCI Telecom Mezzanine Card
MSA SFP	MultiSource Aggreement SFP
RFC 1483	Multiprotocol Encapsulation over AAL5
RFC 1577	Classical IP and ARP over ATM
RFC 1619	PPP over SONET/SDH
RFC 1661	The Point-to-Point Protocol (PPP)
RFC 1662	PPP in HDLC-like Framing
RFC 2474	Definition of the Differentiated Services Field in the IPv4 and IPv6 Headers
RFC 2475	An Architecture for Differentiated Services
RFC 2615	PPP over SONET/SDH
RFC 2684	Multiprotocol Encapsulation over AAL5
ITU-T I.432	B-ISDN User-Network Interface
ITU-T I.363.1	B-ISDN ATM Adaptation Layer Type 1
ITU-T I.363.2	B-ISDN ATM Adaptation Layer Type 2
ITU-T I.363.5	B-ISDN ATM Adaptation Layer Type 5
ITU-T I.366.1	Segmentation and Reassembly Service Specific Convergence Sublayer for the AAL type 2
ITU-T I.610	B-ISDN Operation and Maintenance Principles and Functions
ITU-T G.703	Physical/electrical Characteristics of Hierarchical Digital Interfaces
ITU-T G.707	Network Node Interface for the Synchronous Digital Hierarchy (SDH)
ITU-T G.781	Synchronization Layer Functions
ITU-T G.783	Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks
GR-253-CORE	SONET Transport Systems: Common Generic Criteria.
GR-1244	Clocks for the Synchronized Network: Common Generic Criteria
ATM Forum TM4.1	Traffic Management

Why choose XS-155 ?

XS-155: A Flexible Solution

XS-155 brings even more flexibility to the concept of PMC with the use of a network processor which is entirely re-configurable to support new standards. The PTMC standard adds modularity to the way building blocks are connected together at the system level. The use of SFP optical transceivers also gives flexibility to the user since the connector type can be chosen on a per application basis without any hardware modification.

XS-155: A High Performance Solution

XS-155 architecture improves the overall throughput by segmenting and reassembling packets on the PMC itself. This allows maximizing PCI bandwidth and reaching performance levels that are impossible to achieve on conventional designs. As all the resources are dedicated for the ATM and IP traffic in a deterministic way, XS-155 data rates are more reliable, resulting in better quality of service.

XS-155: A Scalable and Coherent Solution

XS-155 is the first member of a family of interfaces implementing data rates from E1/T1 to OC-12 and Gigabit Ethernet, all using the same architecture, thus giving the same look and feel to the user.

XS-155: A Modern Solution

Xalyo Systems' ATM and IP interfaces are based on a leading edge network processor handling all the data path in hardware while the control path is handled by a processor running VxWorks® or LINUX. An open API is provided on the PCI bus which makes the solution plug and play on virtually any platform, any processor, and any operating system.

Ordering Information

XS-155-4	4 ports, 200 MHz, 384 MB SDRAM, 16 MB Flash
XS-TP001	OC-3/STM-1 multi mode SFP transceivers
XS-TP002	OC-3/STM-1 single mode IR SFP transceivers
XS-TP003	OC-3/STM-1 single mode LR SFP transceivers

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